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Journal of the European Ceramic Society 27 (2007) 4011-4015

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# 1/f electrical noise due to space charge regions

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Available online 26 March 2007

## Abstract

This paper shows how a backgating noise coming from boundary space charge regions becomes a 1/*f* resistance noise due to the biasing of the samples. This overseen noise that is Lorentzian with no bias applied, becomes a continuous set of Lorentzian terms in biased samples that synthesizes a 1/*f* resistance noise. The ratio  $f_{high}/f_{low}$  for the frequency band where 1/*f* noise appears is an exponential function of the bias voltage measured in thermal voltage units  $V_T = kT/q$  at the temperature *T* of the experiment. Grain boundaries and planar interfaces are powerful sources of this 1/*f* electrical noise.

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Keywords: Electrical properties; Dielectric properties; Grain boundaries; Surfaces; Electrical noise

# 1. Introduction

The high gain of GaAs photoconductors at low illumination levels has been explained by the variation of conductive volume taking place in thin epitaxial layers due to transversal photovoltages developed at boundary space charge regions (BSCR).<sup>1,2</sup> This photoconductance gain is a photo-backgating effect from their BSCRs and the evaluation of its signal to noise ratio has lead us to discover an overseen resistance noise in resistors that is the thermo-backgating effect from surrounding or embedded BSCRs that exist at boundary interfaces as the surface or the substrate-epilayer interface of devices and around embedded dislocations and inter-grain boundaries in the material. Two BSCR contributing to the above gain were found in Ref. 2, one in the bottom interface between the conducting film and the substrate and the second aside the surface on top. For this "photo-topgating" gain, a 1/f noise has been demonstrated recently in epitaxial GaAs resistors by optically induced fluctuations of their surface charge diffusing over their surface.<sup>3</sup> This produced a set of random modulations in the channel, each with a 1/f spectrum, giving a 1/f resistance noise in the channel by field-effect. In this way, a 1/f resistance noise in the bulk was produced tracking a surface effect, thus without contradicting a well-known paper of Hooge.<sup>4</sup>

0955-2219/\$ - see front matter © 2007 Elsevier Ltd. All rights reserved. doi:10.1016/j.jeurceramsoc.2007.02.098 Although the above effect is a first reason to expect 1/*f* noise in resistors and granulated materials, the most powerful source of 1/*f* resistance noise is one advanced at the end of Ref. 3, due to the interaction of BSCRs with the bias applied to the sample, that leads to a 1/*f* noise synthesised by a set of Lorentzian terms detuned and weighted as required to generate a 1/*f* spectrum, as this paper shows for the first time.

#### 2. Space charge voltage noise (SCV noise)

This section shows that a BSCR uses to be a trembling boundary for the resistor that it limits due to the thermal fluctuation of electrostatic energy stored in such BSCR. To show this important result, let us consider first the thermal noise of a resistance *R* at temperature *T*, shunted by a capacitor *C*. As it was known some time ago,<sup>5</sup> the flat noise power density  $S_V(f) = 4kTR (V^2/Hz)$  of *R* (its Johnson noise) being filtered by *C* produces a Lorentzian spectrum in the form:

$$S_{\rm V}(f) = \frac{4kTR}{1 + (f/f_{00})^2} = \frac{4kT}{2\pi C} \frac{f_{00}}{f^2 + (f_{00})^2} \tag{1}$$

whose total power is  $\langle v_n^2 \rangle = kT/C(V)^2$  no matter the *R* value considered. This striking property leads to the so-called kT/C noise of capacitance-based devices as CCDs.<sup>6</sup> Thus, capacitance, temperature and Boltzmann's constant *k* set the mean squared voltage fluctuation  $\langle v_n^2 \rangle$  that will exist in any capacitance *C* from thermodynamical reasons, because this kT/C noise power is the same for a capacitance of *C* pF shunted by few k $\Omega$ 

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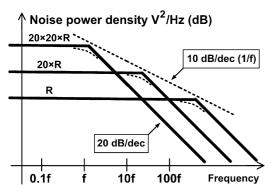


Fig. 1. Bode plots of the Lorentzian voltage noise existing in an R-C parallel circuit for different resistance values shunting the same capacitance C.

(a leaky capacitor) than for a capacitance of the same value shunted by billions of  $G\Omega$  (a high quality capacitor).

What changes is the spectral distribution of the above power, that will be a high-amplitude, narrow band, Lorentzian spectrum for a good capacitor and a low-amplitude Lorentzian noise covering a much higher bandwidth from  $f \rightarrow 0$  (dc) to  $f_{00} = 1/2\pi RC$  Hz for the leaky capacitor. Perhaps a "lifetime"  $\tau = RC$  sounds better to deal with these first-order, low-pass (Lorentzian) spectra, as those that appear in the Bode plots of Fig. 1 for three capacitors of the same capacitance C shunted by "leakage" resistances R, 20R and 400R. The kT/C noise power conservation leads to three Lorentzian terms whose low-frequency flat amplitude is inversely proportional to their cut-off frequency  $f_{00}$ , thus aligning the corners of these Lorentzian terms along the 1/f dashed line (10 dB/dec power roll-off) as shown in Fig. 1. This feature will lead to synthesize 1/f noise from the sum of logarithmically spaced Lorentzians forming a ladder with constant step height as in Fig. 1. This kT/C noise will exist in any capacitance C no matter the mean (dc) voltage it stores. Any physical structure able to store electrostatic energy as a parallel-plate capacitor or a junction capacitor with  $R \neq 0$ , also will have this voltage noise.

Let us consider the metal–semiconductor (Schottky) diode whose cross-section appears in Fig. 2, where the upper metallic contact G is a metal electrode (gate) placed onto a semiconductor (SC) layer that will be assumed to be n-type, thus converting

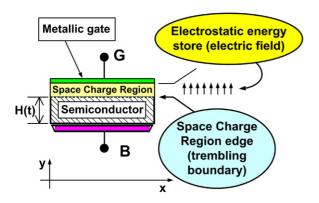


Fig. 2. Schottky diode viewed as a planar interface with a space charge region that stores electrostatic energy in the electrical field existing between the metal gate (G) and the equipotential semiconductor accessed through contact B as described in the text. Under open circuit conditions, the SCR thickness H(t) fluctuates slightly due to the kT/C noise of the diode.

the gate in the anode and the bottom contact B in the cathode of the diode. This contact is the *best ohmic contact* (BOC) for the SC region because other ohmic contacts in this region (e.g. coplanar ones with the gate) lead to lateral access resistances harmful at high frequencies<sup>7</sup> for example. This BOC helps to make equipotential the SC bulk (cathode) as it also is the metallic anode.

Due to the space charge region between the SC layer and the metal of this diode, its equivalent circuit under thermal equilibrium (TE) will be a capacitance C between B and G terminals shunted by some resistance R. As it was shown in Ref. 2 the R value to be used for small signals as electrical noise is the dynamical resistance of the diode  $r_{d}(v)$  that is an exponential function of any quiescent voltage v existing in the junction, as the photovoltages that flattened the Arrhenius plots of Ref. 2. Hence, the voltage noise signal existing in TE between B and G terminals will show a Lorentzian spectrum with a cut-off frequency  $f_{00} = 1/2\pi r_d C$  as those of Fig. 1. From the typical *i*-v characteristic of a Schottky diode, it can be shown that tens of mV dc existing in such diode are enough to shift clearly both the cut-off frequency  $f_0(v)$  and the amplitude of its Lorentzian SCV *noise*. For such low biasing, the capacitance of the diode C(v)can be taken as constant, but this is not the case for its dynamical resistance  $r_{\rm d}(v)$ . Using this *i*–*v* characteristic:

$$i = I_{\text{sat}}\left(\exp\left(\frac{v}{V_{\text{T}}}\right) - 1\right) = I_{\text{sat}}[\exp(u) - 1]$$
(2)

where  $u = v/V_T$ , v being the bias voltage and  $V_T = kT/q$  the thermal voltage unit (26 mV at room temperature). The dynamical resistance of the diode is:

$$r_{\rm d}(v) = \left(\frac{\partial i}{\partial v}\right)^{-1} = \frac{V_{\rm T}}{I_{\rm sat}} \exp(-u) = r_{\rm d0} \exp(-u)$$
(3)

It is worth noting that p–n junction diodes made from Si or GaAs, use to have  $r_{d0}$  values in the  $10^{12} \Omega$  range, making them very difficult devices to be handled properly by a sensing electronics, but Schottky diodes, with much lower built-in voltages  $V_{bi}$  than such p–n diodes, can be handled with acceptable loading effects by a sensing electronics having  $100 \text{ M}\Omega$  or higher input impedance, as that of a low-noise EGG-PAR Model 113 pre-amplifier (LNA).

From Eq. (3), a small reverse bias v = -75 mV sets the dynamical resistance of the diode to a 20 times higher value  $(20r_{d0})$  than it was in TE, while its capacitance remains roughly the same. This allows writing the cut-off frequency of the Lorentzian spectrum of the so-called *kT/C* noise in our Schottky diode as:

$$f_0(u) = \frac{1}{2\pi C r_{\rm d}(u)} = \frac{1}{r_0 C} \exp(u) = f_{00} \exp(u) \tag{4}$$

Eq. (4) predicts an electrical tuning of  $f_0$  in the diode by the applied bias v that will be accompanied by a change in the amplitude of its kT/C or SCV noise as it is shown in Fig. 1. Like this Schottky diode, any boundary space charge region will be a source of Lorentzian noise whose lifetime will be tuned electrically by the bias existing in such interface. For similar reasons, the temperature T also will tune this SCV noise spectrum J.I. Izpura / Journal of the European Ceramic Society 27 (2007) 4011-4015

and moreover, its lifetime will appear as *thermally activated* with energy  $E_{\rm T} \approx q V_{\rm bi}$ , where q is the electronic charge and  $V_{\rm bi}$  is the built-in voltage of the junction. This behaviour comes from the exponential dependence of  $r_{\rm d0}$  with the energy  $E_{\rm T}$ , a fact exploited in Ref. 2 to obtain surface band-bendings by photoconductance measurements.

We have to be very cautious with this tuning feature, however, because any bias voltage  $v = V_Q$  between B and G terminals will take the diode out of TE, thus setting some bias current  $I_{\rm O}$  (reverse or forward) across the diode whose shot noise will add to the Johnson noise of any *leakage resistance*  $R_{\text{leak}}$ assumed in the diode to "justify" its kT/C noise. This  $R_{\text{leak}}$ always can be assumed in parallel with  $r_{\rm d}(v)$  to have a kT/Cnoise that is  $\langle v_n^2 \rangle = kT/C(V)^2$  no matter the R value used. Taking  $R_{\text{leak}} = 10^{30} \Omega$  that means  $R \to \infty$  from a practical viewpoint, we justify the existence of kT/C noise in the diode due to its R-Crelaxing cell, *besides* the shot noise due to  $I_{\Omega}$ . This shot noise that is a broadband noise due to the short transit time of carriers across the junction, will add in power (uncorrelated) to the Johnson noise of  $R_{\text{leak}}$ . The final result is a unique noise spectrum shaped by C and  $r_d(v)$  (Lorentzian) comprising both the kT/C noise due to  $C(V^2)$  and the contribution of this shot noise  $2qI_{O}(A^{2})$  once converted to voltage noise  $(V^{2})$  through  $[r_{d}(v)]^{2}$ .

## 3. Experimental proof of SCV noise in Schottky diodes

To show how the Lorentzian noise spectrum of an interface is tuned by its own bias voltage  $v = V_0$ , a commercial BAT85 Si-Schottky diode was used. From the forward voltage  $V_{\rm f} = 235 \,\mathrm{mV}$ measured in this diode at room T ( $V_T = 25.9 \text{ mV}$ ) while its dc current was  $I_{\rm f} = 1.23$  mA, Eq. (2) gives:  $I_{\rm sat} = 1.4 \times 10^{-7}$  A and  $r_{d0} = 185 \text{ k}\Omega$  that allow to design the circuit of Fig. 3. For C = 10 pF from the BAT85 datasheets, we have:  $\tau_0 = 1.85 \text{ }\mu\text{s}$  or  $f_{00} = 86$  kHz. This high *native*  $f_{00}$  was lowered to  $f_{01} = 183$  Hz by a high quality capacitor of 4700 pF in parallel with the BAT85. This  $f_{01}$  is well suited to the input characteristics of our LNA and below 25 kHz, the cut-off frequency of the anti-aliasing filter of our noise meter described in Ref. 3. This high capacitance in parallel also makes unimportant any small change of C with  $V_{\rm O}$ , a beneficial feature used in Ref. 2 to measure comfortably the thermal activation energy  $E_{\rm T} \approx q V_{\rm bi}$  of  $r_{\rm d}(V_{\rm O})$  in GaAs Schottky junctions.

Fig. 3 shows the circuit used to measure voltage noise in the BAT85 biased by a small battery ( $V_{CC}$ ) enclosed in the shielded test fixture. It offers a rather high resistance  $R_L \approx 1 \text{ M}\Omega$  in parallel with the expected  $r_{d0} = 185 \text{ k}\Omega$ , thus producing a low loading effect on our "*C*-enhanced" diode. The switch allows to change the reverse bias voltage of the diode from  $V_Q \approx -V_T$  to  $-7V_T$ , as it can be seen in Table 1, where also are shown two voltages  $V_A$ 

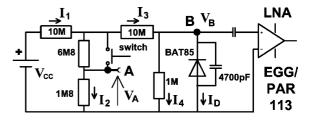


Fig. 3. Electrical circuit used to tune and measure noise in a BAT85 Schottky diode.

and  $V_B$  measured on the circuit with a Keithley-195A voltmeter (1 G $\Omega$  load resistance) that allow to calculate the currents given there. The corresponding dynamic resistances  $r_d$  of the diode for these  $V_Q$  values and for  $V_Q = 0$  ( $V_{CC} = 0$ ) appear in Table 2 together with the cut-off frequencies  $f_0(V_Q)$  they would give for the noise spectra of the diode shunted by the fixed capacitor, without the load of the bias circuit in parallel that starts to dominate when  $r_d(V_Q)$  becomes similar to (or higher than)  $R_L \approx 1 M\Omega$ .

Table 2 also shows the theoretical cut-off frequencies  $f_0^{\#}(V_Q)$ resulting from this loading effect as well as the experimental cut-off frequencies  $f_0^{@}(V_Q)$  extracted from the noise spectra of Fig. 4 that were measured in the circuit for the above  $V_{\rm O}$  values. As it can be seen, the measurements agree well with the theoretical predictions of Eqs. (1) and (4). Curve (a) in Fig. 4 is the noise spectrum measured in the circuit of Fig. 3 with the input of the LNA shorted, thus being a reference about the lowest power spectral density (in V<sup>2</sup>/Hz) that our system can handle due to the equivalent input noise  $(e_n)^2$  of the rather old LNA. Curves (b)-(d) are three Lorentzian spectra measured for  $V_{\rm Q} = 0$ ,  $-V_{\rm T}$  and  $-7V_{\rm T}$ . Curve (e) is a final check that revealed that shot noise also was present. This curve is the noise measured in the circuit with both the BAT85 and the  $4700 \, pF$  capacitor removed and  $V_{CC} = 0$ . It was done to check this reasoning: since  $r_d(-7V_T) = 200 \text{ M}\Omega$  vanishes in parallel with  $R_{\rm L} \approx 1 \,\mathrm{M}\Omega$ , the flat part of curve (d) would have to be equal to that of curve (e). But the flat part of curve (d) at  $S_n \approx -129 \text{ dB}$  $(1.26 \times 10^{-13} \text{ V}^2/\text{Hz})$  is 8.8 dB over curve (e), the familiar thermal noise of a 1 M $\Omega$  resistor (-137.8 dB or 1.66  $\times$  10<sup>-14</sup> V<sup>2</sup>/Hz) often used to test the system and whose drop around 6 kHz is due to the 25 pF capacitance at the input of the LNA.

Thus, there is more noise in curve (d) than the expected from the above reasoning and the reason is that, although  $r_d(-7V_T) = 200 \text{ M}\Omega \text{ vanishes}$  in parallel with  $R_L \approx 1 \text{ M}\Omega$ , the shot noise of  $I_d(-7V_T)$  and  $I_4$  does not vanishes at all and its power spectral density:  $2q(I_d + I_4) = 1.3 \times 10^{-25} \text{ A}^2/\text{Hz}$  will be converted by  $|Z(j\omega)|^2 \approx (R_L)^2$  to a voltage power density. This gives:  $1.3 \times 10^{-13} \text{ V}^2/\text{Hz}$  that will add in power with the thermal noise of  $R_L$ , thus giving  $S_n(f < 34 \text{ Hz}) = 1.4 \times 10^{-13} \text{ V}^2/\text{Hz}$ 

Table 1 Measured voltages and calculated currents in the circuit of Fig. 3

		U					
$V_{\rm CC} = 12.38  {\rm V}$	$V_{\rm A}$ (V)	$V_{\rm B}~({ m V})$	<i>I</i> <sub>1</sub> (µA)	<i>I</i> <sub>2</sub> (µA)	<i>I</i> <sub>3</sub> (µA)	<i>I</i> <sub>4</sub> (µA)	$I_{\rm d}$ ( $\mu$ A)
Switch ON	1.630	0.025	1.075	0.906	0.169	0.025	0.144 0.208
Switch OFF	0.818	0.185	0.847	0.454	0.393	0.185	0

#### Table 2

Theoretical and experimental cut-off frequencies for the noise spectra of the BAT85 Schottky diode under three quiescent bias voltages

Bias V <sub>Q</sub>	$r_{\rm d0}~({ m M}\Omega)$	$f_0$ (Hz)	$f_0^{\#}$ (Hz)	$f_0^@$ (Hz)
0	0.185	183	217	190
$-V_{\mathrm{T}}$	0.500	68	101	90
$-7V_{\rm T}$	200	0.17	34	35

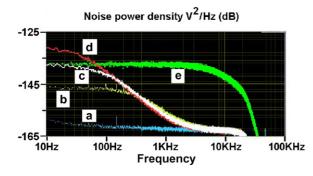


Fig. 4. Noise spectra measured in the circuit of Fig. 3 under these conditions: (a) diode replaced by a short circuit; (b)  $V_{CC} = 0$  and switch OFF; (c) switch ON; (d) switch OFF; (e) both diode and capacitor removed.

(-128.5 dB) for curve (d) that explains perfectly the extra noise found in the reverse biased diode. Therefore, planar junction diodes are generators of Lorentzian noise that are tuned by small bias voltages  $V_Q \approx V_T$ . This noise includes both the *kT/C* noise of the diode capacitance existing in TE ( $V_Q = 0$ ) as well as the shot noise of any current existing in the diode for  $V_Q \neq 0$  V.

# 4. From SCV noise (in $V^2)$ to interface induced thermal noise (in $\Omega^2)$

Once the SCV noise existing at interfaces has been shown, let us show its effect on the sheet resistance of conducting layers parallel to them. Going back to Fig. 2, the thickness H of the SC layer will be modulated by the SCV noise of the interface, thus being a function of time H(t). This follows from the finite doping  $N_{\rm D}$  of the SC leading to a varying depletion layer width to track the SCV noise. In Fig. 5 derived from Fig. 2, the SC layer used as a conducting channel without the BOC and with two new ohmic contacts Source S and Drain D placed at its ends, actually is a field-effect transistor (FET) whose gate-channel capacitance has a small voltage signal due to its SCV noise. This small signal will modulate the channel thickness H(t) by the well known field-effect, thus producing a resistance noise in the channel mirroring the SCV noise. To say it bluntly: the resistance between terminals S and D in Fig. 5 is not constant. Instead it has a mean value  $R_{ch}$  together with a resistance noise of zero mean and Lorentzian power spectrum (in  $\Omega^2$ ) tracking the SCV noise of the BSCR parallel to the channel.

Thus, a conducting channel bounded by a floating gate will have an interface-induced thermal noise (IIT noise shortly). This floating gate FET device (FGFET) is very likely to be found because thin-film resistors for example use to have a substrate on which they lie. Their substrate/thin-film heterojunction uses

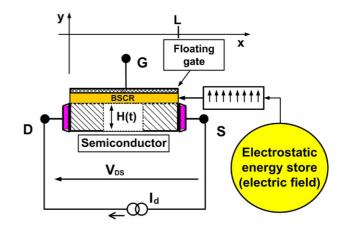


Fig. 5. Planar interface whose space charge region is parallel to the semiconductor region used as a resistor channel whose thickness H(t) will fluctuate due to the kT/C noise of such interface being a BSCR (see text).

to have a space charge region to equalize Fermi levels and *this converts the substrate into a disturbing floating gate* for the thinfilm resistor, because the substrate conductivity is not null and its thickness uses to be high. From all the above, we would have to pay attention to these FGFET devices in any planar device we can make and especially in materials plenty of grain boundaries or dislocations.

All the above suggests that a Lorentzian IIT noise coming from interfaces under TE would have to be observed quite often, a feature that seems to be in conflict with the *1/f electrical noise* widely found that seems quite different. To solve this conflict, let us consider the traditional method used to measure resistance noise by a dc current  $I_d$  flowing through the sample to convert any channel resistance fluctuation into a voltage fluctuation between D and S terminals, able to drive a spectrum analyzer not designed to measure resistance noise directly. This method leads to a dc voltage  $V_{DS}$  along the channel that will drop linearly along the resistor for  $V_{DS}$  values low enough to avoid noticeable pinch-off effects in the channel. Let us take  $V_{DS} = 6V_T \approx 150$  mV in Fig. 5 to obtain some numerical results.

With the above  $V_{\text{DS}}$  applied, the floating gate will acquire a floating voltage  $0 < v_{\text{float}} < V_{\text{DS}}$ , thus leaving part of the Schottky junction forward biased (in the source side) while the remaining part becomes reverse-biased, *in such a way that the opposed injection and extraction currents flowing through each part of the junction cancels one to each other*, to make null the *net* charge transfer from the resistor to its floating gate. This dynamic equilibrium and Eq. (2) lead to:  $v_{\text{float}} = V_{\text{T}} \ln[U_d/1 - \exp(-U_d)]$  where  $U_d = V_{\text{DS}}/V_{\text{T}}$ .<sup>8</sup> Thus the floating gate acquires a voltage  $v_{\text{float}} = 1.8V_{\text{T}} \approx 45 \text{ mV}$ , and the gate-source bias voltage of the FGFET in Fig. 5 is:  $V_{\text{GS}} = 45 \text{ mV}$  while its gate-drain bias voltage becomes  $V_{\text{DS}} = -105 \text{ mV}$ . This produces *a non-uniform bias of the Schottky junction along the channel*, where there is a voltage drop  $V_{\text{DS}} = 6V_{\text{T}}$  while  $I_d$  flows.

Considering the channel of Fig. 5 as formed by several slices or small Schottky diodes connected in series along the *x* axis, the SCV noise on the first slice aside the drain will be a Lorentzian one as the one labelled  $20 \times 20R$  in Fig. 1 with  $f_{low}$  as its cut-off frequency, but the SCV noise of the last slice aside the source will be the Lorentzian labelled *R* in Fig. 1, thus having a cutoff frequency  $f_{high} = f_{low} \exp(6) \approx 403 f_{low}$ . And there will be a continuous set of intermediate SCV noises for the inner slices, like the one labelled 20*R* in Fig. 1, but with cut-off frequencies covering all the bandwidth ( $f_{low} - f_{high}$ ), that approaches three decades for this rather low  $V_{DS}$ . The sum of this continuous distribution of Lorentzian terms synthesises 1/*f* noise in the band ( $f_{low} - f_{high}$ ) as the Bode plots of Fig. 1 sketch quite neatly, but those readers not familiar with Bode plots may prefer to look at Fig. 1 in Ref. 9. The mathematical work of this synthesis process that we propose here will be published elsewhere,<sup>8</sup> but the reader can get an advanced idea from the McWorther or Dutta–Horn models shown in Ref. 9 for carrier traps, *thus in a very different context than the electrical one we are using*.

Hence, researchers using the method based on  $I_d$  to observe resistance noise in channels with unintentional but unavoidable BSCRs, will not find a Lorentzian IIT noise tracking the SCV noise of Eq. (1) because their samples are taken out of *TE by I*<sub>d</sub>, injected with Ohm's law in mind to convert IIT noise into voltage noise emerging over the Johnson noise of the mean channel resistance  $R_{ch}$ . Instead, they will find a sum of Lorentzian noises (logarithmically spaced due to the linear drop of  $V_{DS}$ ) viewed as a 1/*f* noise over a broad band that comes from the interaction of those BSCRs with the applied bias during the measurement. As it is shown in Ref. 8, most of the 1/*f* electrical noise found by researchers comes from this hidden feature of actual resistors: their non-constant resistance due to unintentional but unavoidable floating gates in their vicinity.

# 5. Conclusions

Backgating effects from double layers surrounding conductors or embedded in their volume have not been considered from the noise viewpoint. This gives a thermally unstable character to some boundaries in conductors that generates a resistance noise (IIT noise). Attempts to convert this IIT noise of samples into a voltage or current noise able to drive a spectrum analyzer, use to scatter the initial IIT noise under TE into a set of Lorentzian noise terms in these samples brought out of TE by such attempts. This set of spectra synthesises a 1/f noise when the bias voltage  $V_{DS}$  parallel to the BSCR surpass some  $V_T$  units. Conductors plenty of BSCR as granulated materials, will be very prone to show this kind of 1/f electrical noise due to the high number of FGFET devices they have embedded. This 1/f electrical noise coming from the interaction of space charge regions with the electrical stimulation of samples would have to be accounted for in the study of other sources of 1/f noise proposed under the approach of a perfectly constant conductive volume for the devices where low-frequency noise is measured.

#### Acknowledgements

The support of the project CTQ2004-02362/BQU of the Spanish CICYT and that of the project PAC-05-001-2 of the Junta de Castilla-La Mancha, is acknowledged.

# References

- Izpura, J. I. and Muñoz, E., Epitaxial photoconductive detectors: a kind of photo-FET devices. In *Proceedings of the IEEE-WOFE'97*, 1996, pp. 73–80.
- Izpura, I., Valtueña, J. F. and Muñoz, E., Surface band-bending assessment by photocurrent techniques. Application to III–V semiconductors. *Semicond. Sci. Technol.*, 1997, **12**, 678–686.
- Izpura, J. I. and Malo, J., 1/f noise enhancement in GaAs. In Proceedings of the 18th International Conference on Noise and Fluctuations (ICNF 2005), AIP Conference, vol. 780, 2005, pp. 113–116.
- 4. Hooge, F. N., 1/f noise is no surface effect. Phys. Lett., 1969, 29A, 139-140.
- Motchenbacher, C. D. and Fitchen, F. C., *Low-Noise Electronic Design*. John Wiley & Sons, New York, 1973.
- 6. Bell, D. A., Noise and the Solid State. Pentech Press, London, 1985.
- Izpura, J. I., Side contact effects on the capacitance properties of junction devices. Application to III-nitrogen structures. *Semicond. Sci. Technol.*, 2001, 16, 243–249.
- Izpura, J. I., 1/f electrical noise in planar resistors: the joint effect of a backgating noise and an instrumental disturbance. *IEEE Trans. Instrum. Meas.*, accepted for publication.
- 9. Raychaudhuri, A. K., Measurement of 1/f noise and its application in materials science. *Curr. Opin. Solid. State Mater. Sci.*, 2002, **6**, 67–85.